WHAT IS CLAIMED IS:

1. A transistor comprising:

a vertical channel protruding from a substrate including a source/drain region junction between the vertical channel and the substrate; and

an insulating layer extending on a side wall of the vertical channel toward the substrate to beyond the source/drain region junction.

2. A transistor according to Claim 1, wherein the insulating layer further extends on a top surface of the channel.

3. A transistor according to Claim 1 further comprising:

a nitride layer extending on the side wall away from the substrate to beyond the insulating layer.

4. A transistor according to Claim 3 wherein the nitride layer is absent from beyond the junction.

5. A transistor according to Claim 3 further comprising:

a second insulating layer extending on the side wall, wherein the second insulating layer is separated from the channel by the nitride layer.

6. A transistor according to Claim 1 further comprising:

a gate electrode extending on the side wall toward the substrate to beyond the source/drain region junction.

7. A transistor according to Claim 1, wherein the channel has a width that gradually increases toward the substrate.

8. A transistor according to Claim 1, wherein the channel has an upper width and a lower width, wherein the upper width of the channel is uniform and the lower width of the channel gradually increases toward the substrate.

9. A transistor according to Claim 1 further comprising:

a mask insulating layer extending on a top surface of the channel.

10. A transistor according to Claim 9, wherein the mask insulating layer comprises an etch stop nitride layer and a pad oxide layer.

11. A transistor according to Claim 10, wherein the mask insulating layer further comprises a pad nitride layer.

12. A transistor according to Claim 9, wherein the mask insulating layer comprises alternating oxide and nitride layers.

13. A transistor comprising:

a plurality of vertical channels protruding from a substrate including respective source/drain region junctions between the plurality of vertical channels and the substrate; and

a plurality of insulating layers extending on respective side walls of the plurality of vertical channels toward the substrate to beyond the respective source/drain region junctions.

14. A transistor according to Claim 13 further comprising:

at least one planar region connected to the plurality of vertical channels.

15. A transistor according to Claim 13, wherein the plurality of insulating layers further extends on respective top surfaces of the plurality of channels.

16. A transistor according to Claim 13 further comprising:

a plurality of nitride layers extending on the respective side walls away from the substrate to beyond the plurality of insulating layers.

17. A transistor according to Claim 16, wherein the plurality of nitride layers are absent from beyond the respective junctions.

18. A transistor according to Claim 16, wherein the plurality of channels are separated by the plurality of nitride layers.

19. A transistor according to Claim 13 further comprising:

a gate electrode extending on the respective side walls of the plurality of channels toward the substrate to beyond the respective source/drain region junctions.

20. A transistor according to Claim 13 wherein the plurality of channels are oriented in a parallel configuration.

21. A method of forming a transistor comprising:

forming a vertical channel protruding from a substrate including a source/drain region junction between the vertical channel and the substrate; and

forming an insulating layer extending on a side wall of the vertical channel toward the substrate to beyond the source/drain region junction.

22. A method according to Claim 21, wherein the step of forming an insulating layer further comprises forming the insulating layer on a top surface of the channel.

23. A method according to Claim 21 further comprising:

forming a nitride layer extending on the side wall away from the substrate to beyond the insulating layer.

24. A method according to Claim 23, wherein the nitride layer is absent from beyond the junction.

25. A method according to Claim 23 further comprising:

forming a second insulating layer extending on the side wall, wherein the second insulating layer is separated from the channel by the nitride layer.

26. A method according to Claim 21 further comprising:

forming a gate electrode extending on the side wall toward the substrate to beyond the source/drain region junction.

27. A method according to Claim 21, wherein the step of forming a vertical channel further comprises:

forming an oxide layer on the channel; and

removing the oxide layer to reduce channel width.

28. A method according to Claim 27, wherein the step of forming an oxide layer is preceded by forming a pad oxide layer and an oxidation mask layer on the channel, and wherein the step of removing the oxide layer further comprises removing the pad oxide layer and the oxidation mask layer.

29. A method according to Claim 21, wherein the step of forming a vertical channel is preceded by forming a mask insulating layer on a substrate.

30. A method according to Claim 29, wherein the mask insulating layer comprises alternating oxide and nitride layers.

31. A transistor comprising:

a fin that is a vertically protruding portion of semiconductor substrate;

a nitride liner formed on lower sidewalls of the fin;

a buffer oxide layer interposed between the lower sidewalls of the fin and the nitride liner;

a gate insulating layer that are formed on upper sidewalls of the fin and connected to the buffer oxide layer;

device isolating layer separated a predetermined distance from the fin by the nitride liner; and

a gate electrode disposed crossing over the fin.

32. The transistor as claimed in claim 31, wherein top edges of the fin are formed rounded.

33. The transistor as claimed in claim 31, wherein a width of the fin gradually increases from top to bottom.

34. The transistor as claimed in claim 31, wherein an upper width of the fin coated with the gate insulating layer is uniform, and a lower width of the fin coated with the buffer oxide layer gradually increases toward bottom.

35. The transistor as claimed in claim 31, wherein the gate insulating layer is conformally formed on the upper sidewalls and a top surface of the fin.

36. The transistor as claimed in claim 31 further comprising a mask insulating layer consisting of a pad oxide layer and an etch mask layer that are sequentially stacked on a top surface of the fin,

wherein the gate electrode crosses over the mask insulating layer.

37. The transistor as claimed in claim 36, wherein the mask insulating layer further comprises a pad nitride layer interposed between the pad oxide layer and the top surface of the fin.

38. The transistor as claimed in claim 31 further comprising a mask insulating layer formed by alternately stacking an oxide layer and a nitride layer on a top surface of the fin, wherein the gate electrode crosses over the mask insulating layer.

39. The transistor as claimed in claim 31 further comprising:

source and drain regions formed in the fin at both sides of the gate electrode; and

a channel region formed in the fin under the gate electrode.

40. A transistor comprising:

a pillar including a couple of planar regions and a plurality of fins connecting the two planar regions that are a vertically protruding portion of semiconductor substrate and separated from each other;

a nitride liner formed under the pillar;

a buffer oxide layer interposed between lower sidewalls of the pillar and the nitride liner;

a gate insulating layer that is formed on upper sidewalls of the pillar and connected to the buffer oxide layer;

device isolation layers separated a predetermined region by the nitride liner on the sidewalls of the pillar; and

a gate electrode disposed crossing over the fins.

41. The transistor as claimed in claim 40, wherein top edges of the fin are formed rounded.

42. The transistor as claimed in claim 40, wherein a width of the fin gradually increases from top to bottom.

43. The transistor as claimed in claim 40, wherein an upper width of the fin coated with the gate insulating layer is uniform and a lower width of the fin coated with the buffer oxide layer increases toward bottom.

44. The transistor as claimed in claim 40, wherein the gate insulating layer is conformally formed on upper sidewalls and top surface of the pillar.

45. The transistor as claimed in claim 40 further comprising a mask insulating layer consisting of a pad oxide layer and an etch mask layer on top surface of the pillar,

wherein the gate electrode layer crosses over the mask insulating layer.

46. The transistor as claimed in claim 45, wherein the mask insulating layer further comprises a pad nitride layer interposed between the pad oxide layer and a top surface of the pillar.

47. The transistor as claimed in claim 40 further comprising a mask insulating layer formed on the pillar by alternately stacking the oxide layers and the nitride layers,

wherein the gate electrode crosses over the mask insulating layer.

48. The transistor as claimed in claim 40 further comprising:

source and drain regions formed in the pillar at both sides of the gate electrode, respectively; and

a channel region formed in the fins under the gate electrode.

49. A method of fabricating a transistor comprising:

etching a semiconductor substrate to form a fin;

conformally forming a buffer oxide layer and a nitride layer on the semiconductor substrate;

forming an insulating layer thicker than the fin on the semiconductor substrate with the nitride layer;

polishing the insulating layer using chemical-mechanical polishing to expose the nitride layer and to form device isolating layers surrounding the nitride layer;

successively recessing the nitride layer and the buffer oxide layer to form an exposed upper portion of the fin and to form a nitride liner adjacent to the lower sidewalls of the fin;

forming a gate oxide layer on the exposed portion of the fin; and

forming a gate electrode crossing over the fin.

50. A method of fabricating a transistor comprising:

forming a mask insulating layer on a semiconductor substrate;

patterning the mask insulating layer and the semiconductor substrate to form a fin that is a vertically protruding portion of the semiconductor substrate;

conformally forming a buffer oxide layer and a nitride layer on the semiconductor substrate;

forming an insulating layer thicker than the fin on the semiconductor substrate with the nitride layer;

polishing the insulating layer using chemical-mechanical polishing to expose the nitride layer and to form device isolating layers surrounding the nitride layer;

successively recessing the nitride layer and the buffer oxide layer to form exposed upper sidewalls of the fin and to form a nitride liner adjacent to the lower sidewalls of the fin;

forming a gate oxide layer on the exposed upper sidewalls of the fin; and

forming a gate electrode crossing over the fin.

51. A method of fabricating a transistor comprising:

etching a semiconductor substrate to form a pillar including a couple of planar regions and a plurality of fins that connect the planar regions;

conformally forming a buffer oxide layer and a nitride layer on the semiconductor substrate with the pillar;

forming an insulating layer thicker than the pillar on the semiconductor substrate;

polishing the insulating layer using chemical-mechanical polishing to expose the nitride layer and to form device isolating layers surrounding the pillar;

successively recessing the nitride layer and the buffer oxide layer to form an

exposed upper portion of the pillar;

forming a gate oxide layer on the exposed portion of the pillar; and

forming a gate electrode crossing over the fins.

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